Success Story
A Fortune 500 Japan Based Telecom Company

Giga Bit Ethernet MAC Design

The Project

The scope of work for current project is to design a OCP2.0 compliant Gigabit Etherent MAC Controller that supports data transfer speeds of 10/100/1000 Mbps and prototype it on FPGA and then implement it on ASIC. The Gigabit Ethernet MAC controller is designed using Verilog and system verification has to be done using Specimen Elite. The design supports frame address filtering, full duplex & half-duplex mode with CSMA/CD and flow control. The system bus interface is OCP 2.0 level 2.

The Challenge

➢ Development of Gigabit Ethernet MAC for 1000 Mbps data rate
➢ It should support data transfer speeds of 10 Mbps, 100 Mbps, and 1 Gbps in both full and half duplex mode
➢ Media Interface: RGMII and GMII for 1 Gbps and MII for 10 and 100 Mbps
➢ RGMII wrapper to be put separately to reduce pin count
➢ To improve the interfacing system performance by 70 percent

Our Solution

• In house designing of GEMAC from the scratch

• Designed a system which has a capability to configure the interfacing PHY and the system is configured in the run time depending upon the auto-negotiation result.

• Development of DDR (Double Data Rate) IO to generate RGMII interface with reduces the Pin count by 50 percent.

• Automatic checksum generator and the design are made in a way that it can store maximum of 64 packets in one time with check sum calculated. So that there can be a huge data loaded in the FIFO without wasting the FIFO memory.

• A new bus protocol was implemented, which supports very high data rate so that data required for GEMAC operation could be recovered/ loaded in very less time compared to other protocols

• The edge in the interfacing system (firmware) need not to bother about very high efficiency required to generate the checksum required working with IP, UDP and TCP packets.

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Features

Speed and Mode
- 10 Mbps full and half duplex supported
- 100 Mbps full and half duplex supported
- 1000 Mbps full and half duplex supported

Type of Packet Supported
- Jumbo frames supported
- Magic packet supported
- Ethernet packet
- Ethernet type 2
- VLAN supported
- Short frame zero padding supported

Format of packet supported
- Ethernet
- VLAN
- TCP
- IP
- UDP

Data recovery port and data load port
- Supports two OCP slave interface for TX & RX
- Processor interface
- Supports configurable register interface, which can be set by PIO mode
- Supports run time packet based configuration in which each packet can be set for individual checksum calculation, interrupt generation and burst control

Hardware based Checksum support
- Implementation of IP, TCP, and UDP checksum at the hardware side in the transmission path
- In the receiver reception path IP header checksum is validated and checksum for the payload is generated
- In the receiver path detection of IP security packets and encapsulated security payload (ESP) header and authentication header is also done

Benefits

♦ The checksum calculation at the hardware side gives overall system performance improvement by 70 percent. Thus, the system remains almost free even though it is working with transmission/reception of TCP IP and UDP packets.

♦ Supports all types of speeds and operation modes

♦ Supports most of the packet format type. So this reduces load of format conversion from the firmware

♦ It supports 64 packets to be loaded at a time. This reduces load of packet loading from the system bus. Thus, whenever the system bus is free, the firmware can load its entire packet to be transmitted and set the interrupt in the last packet. Once the packet is sent the interrupt will be generated

♦ It supports programmable interrupt sequence, programmable packet numbering interrupt and last data timing interrupt which results decreases the of number of interrupts going to processor and increases performance

♦ Generic configuration of the interfacing PHY is also supported .The firmware can dynamically select different frequency and mode OFF operation and the GEMAC will generate new configuration in the run time and reconfigure the PHY and generate the new auto negotiation result and system will start working on new results.

♦ Network Programs is also supporting force speeds selection by which we can make off the other PHY's on the LAN, which do not support the selected speed

♦ Automatic flow control is also supported. So, if system bus is not free to recover data then GEMAC will automatically send pause frame to the transmitting stations so that the data is not lost

♦ For low power mode independent transmitter and receiver log is supported depending upon the inactivity time setting. These components are set to OFF state

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